IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

WILLIAM B. CONNORS, TERRY E. McMAHON, DONALD W. SCHULTE and KEITH MOORE			HP Docket No. 10007153-1
Serial No.	:	10/003,938	Examiner L. Nguyen
Filed	:	October 31, 2001	Group Art Unit 2853
For	:	CIRCUIT ROUTING FOR PRINTHEAD HAVING INCREASED CORROSION RESISTANCE	

Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

DECLARATION UNDER § 1.131

We declare as follows:

1. We are inventors who, on October 31, 2001, filed the above-identified application. At the time of such invention, we were employees of Hewlett-Packard Company.

2. Prior to July 17, 2001, the patent date U.S. Patent No. 6,260,952, we conceived our invention, and diligently worked toward reducing our invention to practice, as demonstrated by the HP Invention Disclosure, dated September 1, 2000, evidenced by Exhibit 1, which is attached to this declaration.

3. Exhibit 1 indicates conception of a printhead having a circuit with plural resistors and a power source, comprising: a metal stack formed within the circuit and comprised of a first metal layer comprising a power bus coupled to the power source and a second metal layer having a portion that comprises the resistors; at

least one power via formed within the circuit as an interface between the first metal layer and the second metal layer, wherein, at the power via, the second metal layer comprises a separation barrier located adjacent the first metal layer and between at least one resistor of the plural resistors and the power bus; and a controller bus that is connected to the at least one resistor at a controller via, wherein, at the controller via, the second metal layer comprises a separation barrier located adjacent the first metal layer and between the at least one resistor of the plural resistors and the controller bus.

4. Exhibit 1 also indicates conception of a method of manufacturing a circuit for an ink jet printhead, the circuit having plural resistors, a power bus and a controller bus, the method comprising: creating conductive trace routes from the power bus to power vias associated with each resistor and creating conductive trace routes from the power vias associated with each resistor to each resistor and from the controller bus to controller vias associated with each resistor and creating conductive trace routes from the controller vias associated with each resistor to each resistor; and creating a separation barrier to substantially prevent spreading of ink corrosion from the resistors to the power bus and the controller bus, wherein the separation barrier comprises separation barrier portions within the power vias and separation barrier portions within the controller vias.

5. Exhibit 1 also indicates conception of a fluid ejection device comprising: a first metal layer comprising a portion for providing power to a resistor; a non-metal layer overlying the first metal layer and comprising a via; a second metal layer overlying the non-metal layer, conformed with the via and comprising a top conductive layer portion over a bottom layer portion, wherein the bottom layer

portion comprises a resistor and an electrical connection portion, wherein the first metal layer is electrically connected to the electrical connection portion of the bottom layer portion at the via wherein, at the via, the first metal layer is separated from the top conductive layer portion by the electrical connection portion of the bottom layer portion; and a controller bus that is connected to the resistor at a controller via, wherein, at the controller via, the second metal layer comprises a separation barrier located adjacent the first metal layer and between the resistor and the controller bus.

6. Exhibit 1 also indicates conception of a fluid ejection device comprising: a first metal layer comprising a portion for providing power to at least first and second resistors; a non-metal layer overlying the first metal layer and comprising first and second vias corresponding to the first and second resistors; and a second metal layer overlying the non-metal layer, conformed with the first and second vias and comprising a top conductive layer portion over a bottom layer portion, wherein the bottom layer portion comprises first and second resistors and first and second electrical connection portions corresponding to the first and second resistors; wherein the first metal layer is electrically connected to the first electrical connection portion at the first via and the first metal layer is electrically connected to the second electrical connection portion at the second via; and wherein, at the first via, the first metal layer is separated from the top conductive layer portion by the bottom layer portion, and, at the second via, the first metal layer is separated from the top conductive layer portion by the bottom layer portion; and a controller bus that is connected to the first resistor at a first controller via and the second resistor at a second connector via, wherein, at the first and second controller vias, the second

metal layer comprises a separation barrier located adjacent the first metal layer and between the first and second resistors and the controller bus.

7. Exhibit 1 also indicates conception of a method of manufacturing a fluid ejection device, comprising: providing a first metal layer comprising a power bus and a FET bus; providing the second metal layer, a second metal layer comprising a conductive layer portion and a corrosion-resistant layer portion; providing a first electrical connection between the power bus and the second metal layer and a second electrical connection between the second metal layer and the FET bus, wherein the first and second electrical connections are made through the corrosion-resistant layer portion.

8. Exhibit 1 also indicates conception of a fluid ejection device comprising: a first conductive metal layer comprising a first portion for providing control signals to a resistor and a second portion for providing power to the resistor; a second conductive metal layer comprising the resistor, a power portion and a control portion, wherein the control portion is electrically connected to the first portion of the first conductive metal layer through a control via and the power portion is electrically connected to the second portion of the first conductive metal layer through a power via; wherein the second conductive metal layer comprises a corrosion-resistive layer portion, wherein the corrosion-resistive layer portion comprises a first separation barrier, between the control portion of the second conductive metal layer and the first portion of the first conductive metal layer at the control via, and a second separation barrier, between the power portion and the second portion of the first conductive metal layer at the power via.

9. All acts set forth herein and/or relied upon for the purpose of establishing invention prior to July 17, 2001 were carried out in the United States.

10. We declare that all statements made herein of our knowledge are true and all statements made on information and belief are believed to be true. These statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment or both under § 1001 of Title 18 of the United States Code. We understand that such willful false statements may jeopardize the validity of the application or any patent issuing therefrom.

Date: 8-23-2005 William B. Connors
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Date: 8-23-2005
Terry E. McMahon

Date: 8-23-2005
Donald W. Schulte

Date: 8/23/2005
Keith Moore

HEWLETT PACKARD

INVENTION DISCLOSURE

(WKRP document: 20000912.092705)

PDNO: *10007153*	DATE RCVD: *09/12/2000*	ATTORNEY: *TI-M/IJS*

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Initial Information

Descriptive Title of Invention:

A TIJ Vpp Routing Scheme with Superior Resistance to Ink Corrosion

Brief Abstract of Invention: (Please write a brief description of the fundamental invention.)

By placing metal-1 metal-2 Via connections between TIJ resistors and Vpp metal-2 buses, protection against ink corrosion is provided in the form of TaAl in the bottom of the Vias. Current Hippo/Expressa Vpp routing (and to some extent, Zaphod Vpp routing) potentially allows failure of an entire primitive should a single TIJ reistor fail.

Name of Project:

TIJ-3.0

Product Name or Number:

none

Invention History

[redacted]

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.):

Yes. - HP Lab Notebook 10733 (Don Schulte) on pages 49 and 50 (dated 9-1-00).

[redacted]

Exhibit 1

Description of Invention

Please preserve all records of the invention and attach copies

A. Prior solutions and their disadvantages:(if available, attach copies of product literature, technical articles, patents, etc. as attached files in the "Additional Information" section below.)

I'm unaware of prior solutions.

B. Problems solved by the invention:

The potential loss of an entire primitive (10 to 11 resistors) due to catastrophic failure of a single resistor is prevented by this invention, hence, pen reliability is increased.

C. Advantages of the invention over what has been done before:

The invention will improve Print Quality in the event that a blown TIJ resistor allows ink to breach passivation and attack a primitive's primary Vpp metal-2 bus. The invention limits failure to one or two resistors as opposed to failure of an entire primitive (10 to 11 TIJ resistors).

D. Description of the construction and operation of the invention:(include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc. as attached files in the "Additional Information" section below.)

(See electronic attachment) By placing metal-1 metal-2 Via connections between TIJ resistors and metal-2 Vpp buses, the TaAl portion of the metal-2 stack acts as an ink-corrosion barrier at the bottom of the Via, in effect isolating the Vpp bus from exposure to ink.

Party(ies) Involved

Inventor(s):Pursuant to my (our) employment agreement, I (we) submit this disclosure.

Employee Number	Name	Telnet	Location Code
00087106	*Bill Connors*	*715-2912*	*6410-3445*
00305650	*Terry Mcmahon*	*715-1416*	*6410-3445*
00305145	*Donald W Schulte*	*715-1993*	*6410-5331*
00307505	*Keith Moore*	*715-0322*	*6410-3442*

Witness(es):The invention was first explained to, and understood by, me (us) on the following date(s):

Employee Number	Name	Telnet	Date Witnessed
00306736	*Bob Shreeve*	*715-2975*	*Sep/5/2000*
00307627	*Mickey Szepesi*	*715-2562*	*Sep/8/2000*

Additional Information

[redacted]

Project No.
Book J.
TITLE
4

From Page No.

A TIJ 3.x Vpp routing scheme with superior resistance to ink corrosion.

- A potential problem with the present Vpp routing scheme was recently brought to light when a Hippo pen failed in User Rate Testing (URT). A single resistor in primitive 28 blew open and created a breach in the passivation. The ink penetrated the breach and corroded a large portion of the aluminum in the metal-2 Vpp bus. This resulted in a high series resistance (about 300 ohms) on the bus which caused the other resistors in the primitive to fail. Had the Vpp routing scheme described below been utilized on this pen, then only the one TIJ resistor would have failed and Print Quality would have been relatively unaffected.

- It should be possible to create a TIJ 3.x Vpp bus that is more resistant to ink corrosion than the bus schemes which are now in use. This can be done by routing Vpp from pad to primitive in metal-2 and then routing the bus through via-1 to metal-1. The metal-1 bus would supply power, back up through via-1, to the metal-2 TIJ resistors.

- Because the ink is corrosive to the Aluminum portion of the metal-2 AlCu/TaAl stack, it is necessary to isolate the Al in the Vpp bus from the ink. This can be done with the aid of the TaAl portion of the stack, which is relatively unaffected by the ink corrosion. The isolation can be accomplished by making sure that a via, which has a Tantalum barrier that's intrinsic to the metal stack, is between the TIJ resistors and the metal-2 Vpp bus. In the following picture the arrows point to the ink-resistant TaAl barrier that's intrinsic to a metal-1 / metal-2 via.

Figure 1: A cross section of a metal-1 / metal-2 via.

The arrows in this cross-section point to the 'barrier' of TaAl in the bottom of the Via that halts the spread of corrosion.

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Witnessed & Understood by me.	Date	Invented by	Date
9/5/00 09/08/00		Recorded by	9-1-00

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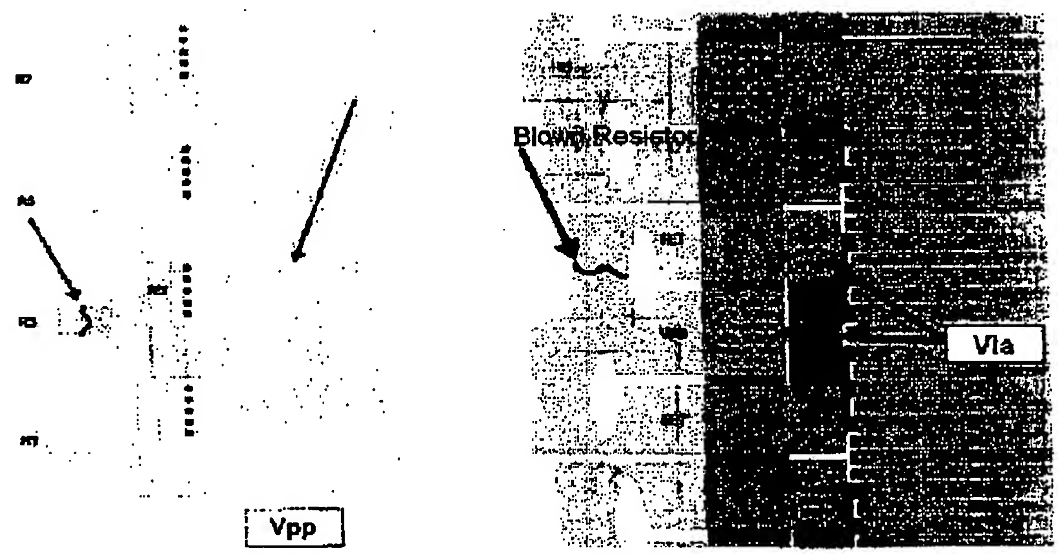
rom Page No. 49

Figure 2: Examples of designs with and without via / TaAl corrosion protection.



The layout on the left shows the Vpp routing scheme that is currently used for Hippo and Expresso (for clarity, only metal-2 is shown). The TIJ resistors and the Vpp bus are both metal-2 and are tied directly together. The arrow on the left points to a blown resistor that has breached the passivation and allowed ink to attack metal-2. Undamaged metal-2 is shown in cyan, corroded metal-2 is shown in yellow The arrow on the right points to the portion of the Vpp bus which has corroded.

The layout on the right shows a portion of the Vpp routing scheme for Zaphod. Metal-2 is shown in cyan, metal-1 is dark blue and corroded metal-2 is yellow. The red arrow points to a blown TIJ resistor which has created a breach in passivation. The aluminum of the surrounding metal-2 stack has been corroded. But the corrosion is unable to travel beyond the Vias because of the TaAl barrier at the bottom of the Vias (see figure 1). Unfortunately, many of the Zaphod TIJ resistors are not protected by vias but are directly tied to the Vpp bus.

Witnessed & Understood by me	Date	Invented by	Date
9/5/00 Michele K. [illegible] 09/08/00			4-1-00
		Recorded by	